AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A multi-chip device comprising:

a group of aligned regions, each region having a programmable interconnection;

a first Integrated Circuit (IC) having a first region of the group of aligned regions;

a second IC having a second region of the group of aligned regions; and

a supporting structure having one or more signal lines, wherein the first region is directly connected to the second region via one of the signal lines, wherein a circuit in the first region is connected to a circuit in the second region without use of any Input/Output (I/O) bank on the first IC.

2. (Original) The multi-chip device of claim 1 wherein the supporting structure comprises a carrier die.

3. (Original) The multi-chip device of claim 1 wherein each region further comprises programmable logic.

4. (Original) The multi-chip device of claim 1 wherein each region of the group of aligned regions on the first IC is substantially identical.

5. (Original) The multi-chip device of claim 4 wherein each region of the group of aligned regions on the second IC is substantially identical.

6. (Original) The multi-chip device of claim 1 wherein the first region includes a line driver and a pad, the pad configured to connect the first region to the second region.

7. (Original) The multi-chip device of claim 1 wherein the second region includes a tile of a field programmable gate array.

8. (Currently Amended) A multi-chip module having:

a first die having a first column of a first plurality of tiles, wherein each tile of the first plurality includes programmable logic;

a second die having a second column of a second plurality of tiles, wherein the second column is aligned with the first column; and

a supporting substrate having a plurality of signal lines, wherein a tile in the first column is directly connected to a tile in the second column via one of the plurality of signal lines and without using any Input/Output (I/O) bank on the first die.

9. (Original) The multi-chip module of claim 8 wherein the tile in the first column comprises a logic block and a switching block.

10. (Original) The multi-chip module of claim 8 wherein the tile in the first column further comprises a line driver and a pad, the pad configured to connect the tile in the first column to the tile in the second column.

11. (Original) The multi-chip module of claim 8 wherein the first die includes configuration logic.

12. (Original) The multi-chip module of claim 8 wherein the first die includes a portion of a programmable logic device.

13. (Original) The multi-chip module of claim 8 wherein the first die and the second die are essentially identical, and wherein the first die has first configuration logic and the second die has second configuration logic.

14. (Original) The multi-chip module of claim 8 wherein the first die and the second die are heterogeneous.

15. (Original) The multi-chip module of claim 14 wherein the first die has programmable logic and the second die has programmable logic and an embedded

application specific integrated circuit (ASIC).

16. (Original) The multi-chip module of claim 14 wherein the ASIC is selected from a group consisting of a microprocessor, a digital signal processor, and an arithmetic processing module.

17. (Currently Amended) A method for creating a multi-chip module (MCM) having a plurality of integrated circuits (ICs), each IC of the plurality of ICs having programmable logic arranged in columns, the method comprising:

positioning a first IC of the plurality of IC's in the MCM, the first IC having a first column of regions, wherein each region has a logic block;

positioning a second IC of the plurality of IC's in the MCM, the second IC having a second column of regions, wherein the second column is aligned with respect to the first column; and

configuring a signal wire to directly connect a first region in the first column to a second region in the second column; and

configuring another signal wire to directly connect a third region in the first column to a fourth region in the second column, wherein the third region is adjacent to the first region, and the fourth region is adjacent to the second region.

18. (Original) The method of claim 17 wherein a logic block in the first region is connected to a logic block in the second region via a line driver.

19. (Cancelled)

20. (Original) The method of claim [[16]] 17 wherein the first IC includes a portion of a programmable logic device (PLD).

21. (Currently Amended) A multi-chip module, having programmable interconnections, comprising;

means for arranging a first plurality of substantially identical connected regions

on a first integrated circuit (IC);

means for arranging a second plurality of substantially identical connected regions on a second IC; and

means for connecting a first region in the first plurality to a second region in the second plurality; and

wherein a first region of the first plurality has means for directly connecting to a second non-adjacent region of the first plurality.

22. (Cancelled)

23. (Original) A system having a plurality of dice, comprising:

a first die of the plurality of dice comprising a first plurality of columns, each column of the first plurality of columns having a first plurality of substantially identical elements;

a second die of the plurality of dice comprising a second plurality of columns, each column of the second plurality of columns having a second plurality of substantially identical elements; and

a plurality of signal lines connecting each element of the first plurality of substantially identical elements of each column of the first plurality of columns with an associated element of the second plurality of substantially identical elements of an associated column of the second plurality of columns.

24. (Original) The system of claim 23 wherein a particular column of the first plurality of columns and the particular column's associated column form an aggregated column of the device.

25. (Original) The system of claim 23 wherein the plurality of signal lines include greater than 100 lines.

26. (Original) The system of claim 23 wherein the plurality of signal lines include greater than 1000 lines.

27. (Original) The system of claim 23 further comprising a carrier die having the plurality of signal lines.

28. (Original) The system of claim 23 wherein each column of the first plurality of columns is filled with the first plurality of substantially identical elements, and each column of the second plurality of columns is filled with the second plurality of substantially identical elements.

29. (Currently Amended) A system having a plurality of dice, the system comprising:

a first die of the plurality of dice, comprising [[first]] all input/output blocks on the first die for communicating with circuits located outside of the first die, and a first function block connected to a first interconnect line;

a second die of the plurality of dice, comprising second input/output blocks for communicating with circuits located outside of the second die, and a second function block connected to a second interconnect line; and

a signal line connecting the first interconnect line to the second interconnect line, wherein a signal propagates from the first interconnect line to the second interconnect line without propagating through any of the [[first]] input/output blocks of the first die.

30. (Previously Presented) The system of claim 29 wherein the signal does not propagate through any of the second input/output blocks of the second die.

31. (Previously Presented) The system of claim 29 wherein the first function block is connected to the second function block via the signal line.

32. (Previously Presented) The system of claim 29 further comprising a carrier die plurality of dice upon which the first die and second die are mounted, wherein the carrier die comprises the signal line.

33. (Previously Presented) The system of claim 29 wherein the first function block

and the second function block are configurable logic blocks.

34. (Previously Presented) The system of claim 29 wherein the first function block is an application specific circuit.

35. (Previously Presented) A multi-chip module having a plurality of dice, the system comprising

a first die of the plurality of dice comprising a first programmable interconnection point connected to a second programmable interconnection point via a first interconnect wire;

a driver connected to the first interconnect wire, the driver not part of an input/output block of the first die;

a second die of the plurality of dice comprising a third programmable interconnection point connected to a fourth programmable interconnection point via a second interconnect wire;

a wire on a third die of the plurality of dice connecting the driver to the second interconnect wire.

36. (Previously Presented) The multi-chip module of claim 35 wherein the driver is relatively smaller than a driver of an input/output block.